Electronic Version

Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A semiconductor wafer comprising:

a silicon substrate with a first region, a second region, and a third region defined on a surface of the substrate, the third region being adjacent to the first region and the second region; and

a capacitor disposed on the substrate, the capacitor comprising:

a first electrode disposed in the first region and the third region on the surface of the silicon substrate;

a first isolation layer covering the first electrode and the silicon substrate; and

a second electrode disposed in the second region and the third region on the surface of the isolation layer.

[c2] 2.The semiconductor wafer of claim 1 wherein the capacitor further comprises a second isolation layer covering the capacitor and the silicon substrate.

[c3] 3.The semiconductor wafer of claim 2 wherein the capacitor further comprises a first contact plug located in the second isolation layer and electrically connected to the first electrode.

[c4] 4.The semiconductor wafer of claim 3 wherein the first contact plug is located in the first region.

[c5] 5.The semiconductor wafer of claim 2 wherein the capacitor further comprises a second contact plug located in the second isolation layer and electrically connected to the second electrode.

[c6] 6.The semiconductor wafer of claim 5 wherein the second contact plug is located in the second region or the third region.

[c7] 7.The semiconductor wafer of claim 1 wherein the semiconductor wafer further comprises a field oxide layer located beneath the first electrode.

[c8] 8.The semiconductor wafer of claim 1 wherein the first electrode comprises a polysilicon layer or a doped polysilicon layer.

[c9] 9.The semiconductor wafer of claim 1 wherein the second electrode comprises a polysilicon layer or a doped polysilicon layer.

[c10] 10.The semiconductor wafer of claim 1 wherein the first isolation layer comprises a silicon oxide layer or a silicon nitride layer.

[c11] 11. A capacitor disposed on a silicon substrate, the silicon substrate with a first region, a second region, and a third region defined on a surface of the silicon substrate, the third region being adjacent to the first region and the second region, the capacitor comprising:
a first polysilicon layer disposed in the first region and the third region on the surface of the silicon substrate;
a dielectric layer covering the first polysilicon layer and the silicon substrate; and
a second polysilicon layer disposed in the second region and the third region on the surface of the dielectric layer.

[c12] 12.The capacitor of claim 11 wherein the capacitor further comprises a first contact plug electrically connected to the first polysilicon layer.

[c13] 13.The capacitor of claim 12 wherein the first contact plug is located in the first region.

[c14] 14.The capacitor of claim 11 wherein the capacitor further comprises a second contact plug electrically connected to the second polysilicon layer.

[c15] 15.The capacitor of claim 14 wherein the second contact plug is located in the second region or the third region.

[c16] 16.The capacitor of claim 11 wherein the capacitor further comprises a field oxide layer located under the first

polysilicon layer.